

TV East/West correction circuit for square tubes

Technology: Bipolar

Features

- Low dissipation
- Square generator for parabolic current specially designed for square C.R.T. correction
- External keystone adjustment (symmetry of the parabola)
- Input for dynamic field correction (beam current change)
- Static picture width adjustment
- Pulse-width modulator
- Final stage D-class with energy redelivery
- Parasitic parabola suppression, during flyback time of the vertical sawtooth

Case: 8 pin dual inline plastic

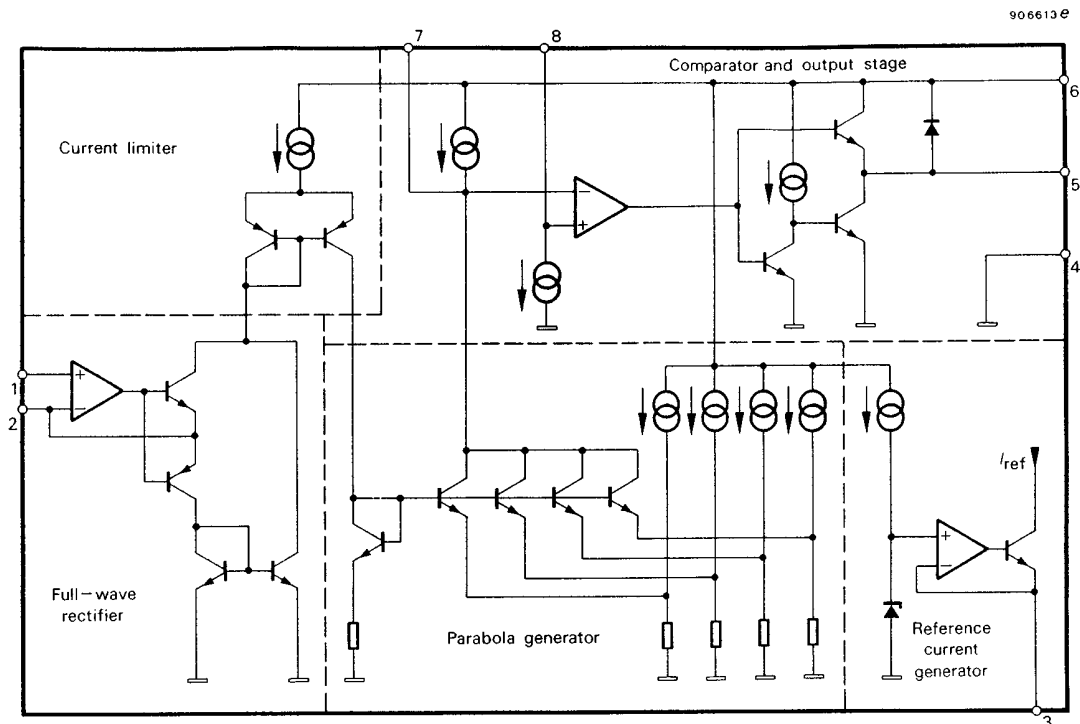


Figure 1 Block diagram

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage Pin 6	V_S	35	V
Supply current Pin 6	I_S	500	mA
Substrate current Pin 5	$-I_5$	400	mA
Power dissipation $T_{case} = 50^\circ\text{C}$	P_{tot}	500	mW
Storage temperature range	T_{stg}	-25 to +150	$^\circ\text{C}$
Junction temperature	T_j	-25 to +150	$^\circ\text{C}$

TDA4950

Electrical Characteristics

$V_S = 26V$, $T_{amb} = 25^\circ C$, Test circuits 1 to 5

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 6	V_S	17	24	30	V
Supply current	Test circuit 1 Pin 6	I_S		4.5	7	mA
Reference voltage	Test circuit 1 Pin 3	V_{ref}	7.6	8.0	8.8	V
Voltage at pin 7 *	$I_{fr} = 0 \mu A$, Test circuit 2 Pin 7	V_{7A}	15.3	16.0	16.7	V
Voltage at pin 7 *	$I_{fr} = 30 \mu A$, Test circuit 2 Pin 7	V_{7C}		15.0		V
Parabola coefficient *	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$	K_1		28		%
Parabola coefficient *	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$	K_2		71		%
Difference *	$V_{DE7} = V_{7E} - V_{7F}$		-40	0	40	mV
Current source	Test circuit 3 Pin 8	I_8		100		μA
Saturation voltage	$I_5 = 400 \mu A$, Test circuit 4 Pin 5	V_{satL}		1	2	V
Saturation voltage	$I_5 = -100 \mu A$, Test circuit 5 Pin 5	V_{satH}		0.8	1.5	V
Forward voltage	$I_5 = 400 \mu A$, Test circuit 5 Pin 5	V_F		1.2	1.7	V
Forward voltage (substrate diode)	$I_5 = -100 \mu A$, Test circuit 4 Pin 5	V_5		0.8	1.2	V

* see figure 2
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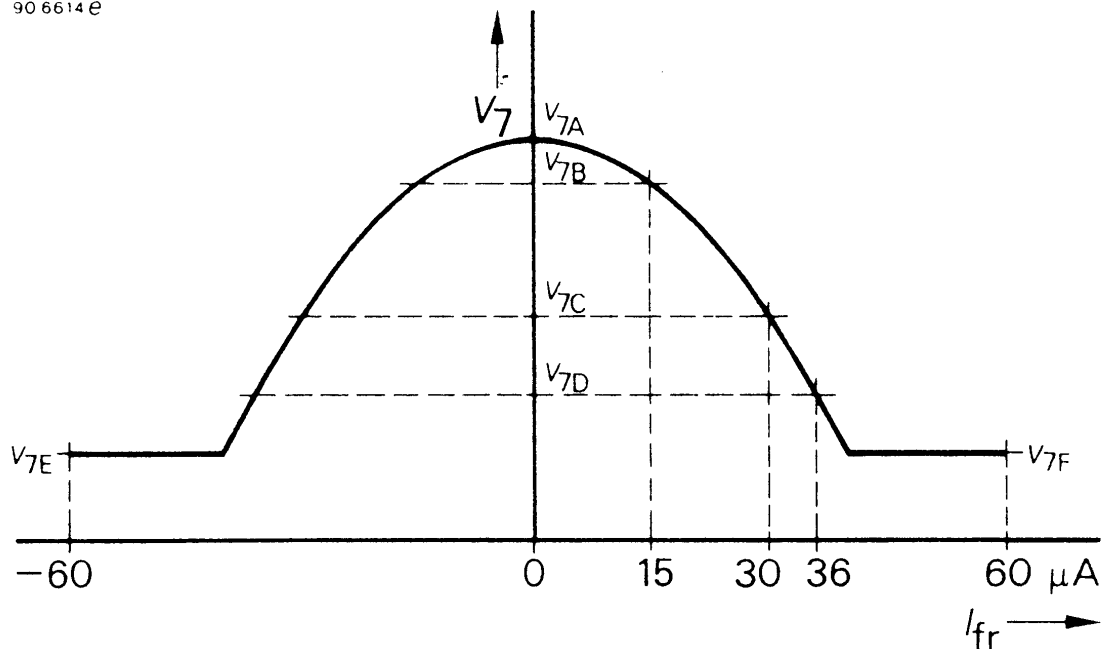
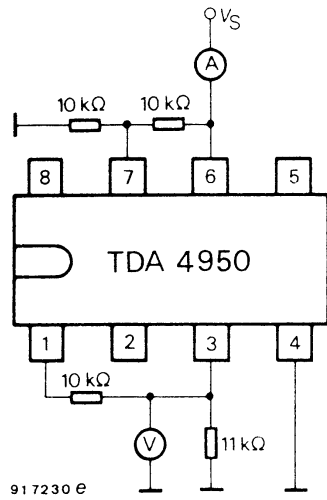
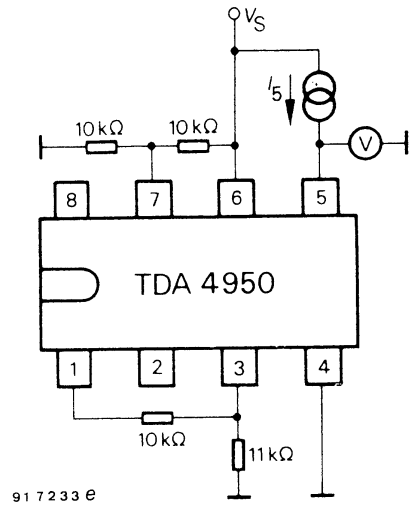


Figure 2 Parabola coefficients



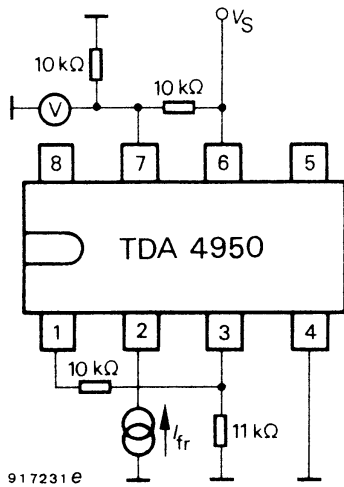
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Figure 3 Test circuit 1



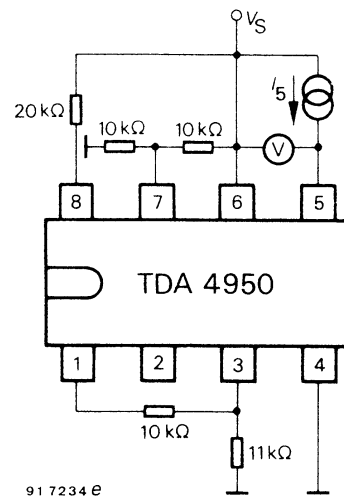
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Figure 6 Test circuit 4



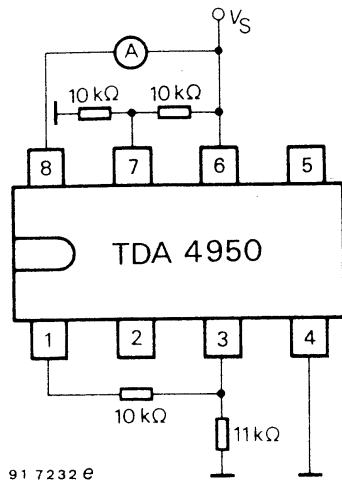
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Figure 4 Test circuit 2



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Figure 7 Test circuit 5

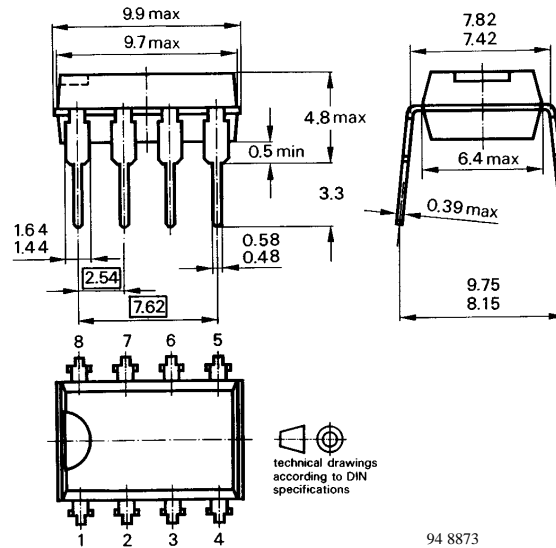


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Figure 5 Test circuit 3

Dimensions in mm

Package: DIP 8



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